STATIC NVRAM WITH ULTRA THIN TUNNEL OXIDES

This application is a Divisional of U.S. Application No. 09/945,398, filed August 30, 2001, now Patent No. 6,730,960 which is a Divisional of U.S. Application No. 09/515,630, filed February 29, 2000, now U.S. Patent No. 6,639,835.

Cross Reference To Related Applications

This application is related to the following co-pending, commonly assigned U.S. patent applications: "Dynamic Flash Memory Cells with UltraThin Tunnel Oxides," serial number 09/513,938, filed Feb. 28, 2000, now U.S. Pat. 6,249,460 and "P-Channel Dynamic Flash Memory Cells with UltraThin Tunnel Oxides," serial number 09/514,627, filed Feb. 28, 2000, now U.S. Pat. 6,384,448, each of which disclosure is herein incorporated by reference. This application is further related to the following co-pending, commonly assigned U.S. patent applications: "Low Voltage PLA's with UltraThin Tunnel Oxides," serial number 09/515,759, filed Feb. 29, 2000, now U.S. Pat. 6,605,961 and "Programmable Low Voltage Decode Circuits with UltraThin Tunnel Oxides," serial number 09/515,115, filed Feb. 29, 2000, now U.S. Pat. 6,351,428, which are filed on even date herewith and each of which disclosure is herein incorporated by reference.

Field of the Invention

The present invention relates generally to semiconductor integrated circuits and, more particularly, to structures and methods for static NVRAM with ultra thin tunnel oxides.

Background of the Invention

The use of the one device cell, invented by Dennard in 1967 (see generally, US Patent 3, 387,286, issued to R. H. Dennard on June 4, 1968, entitled "Field Effect Transistor memory"), revolutionized the computer industry, by significantly